

Fig. 1 (a)

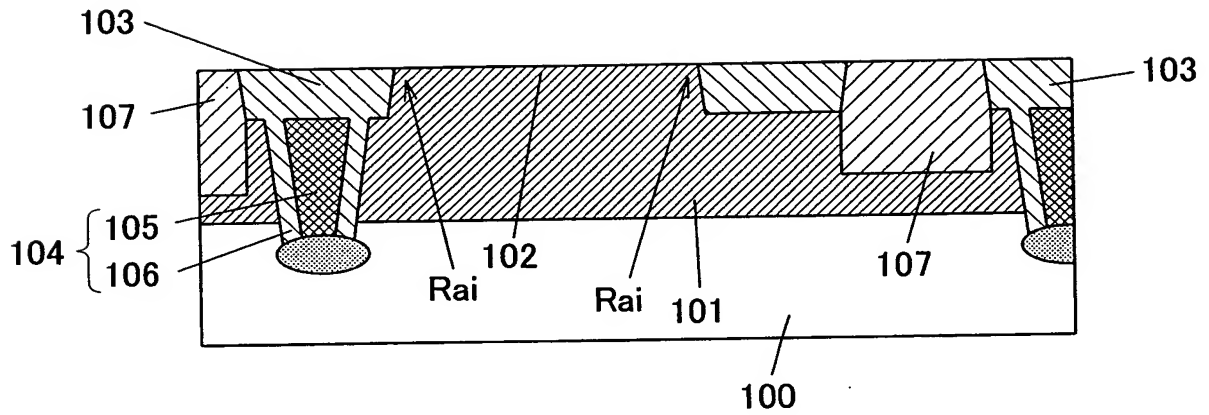


Fig. 1 (b)

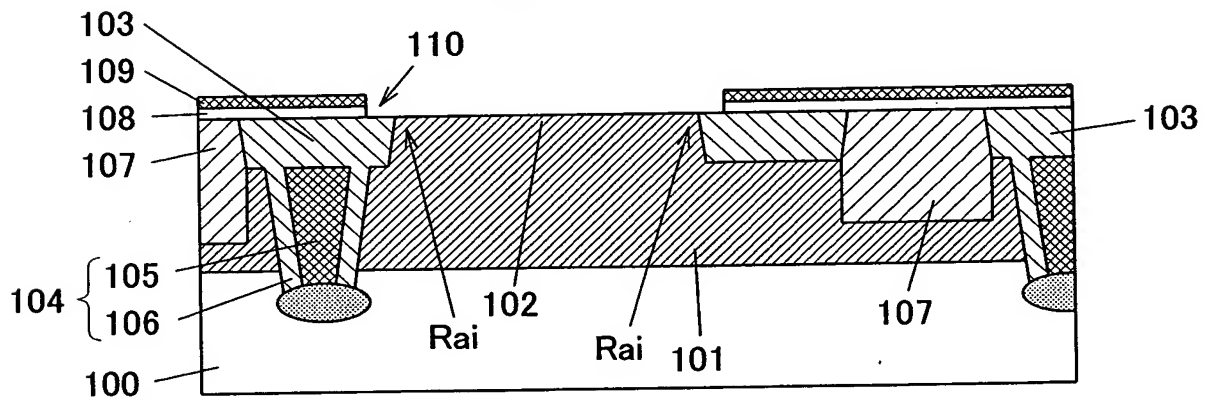


Fig. 1 (c)

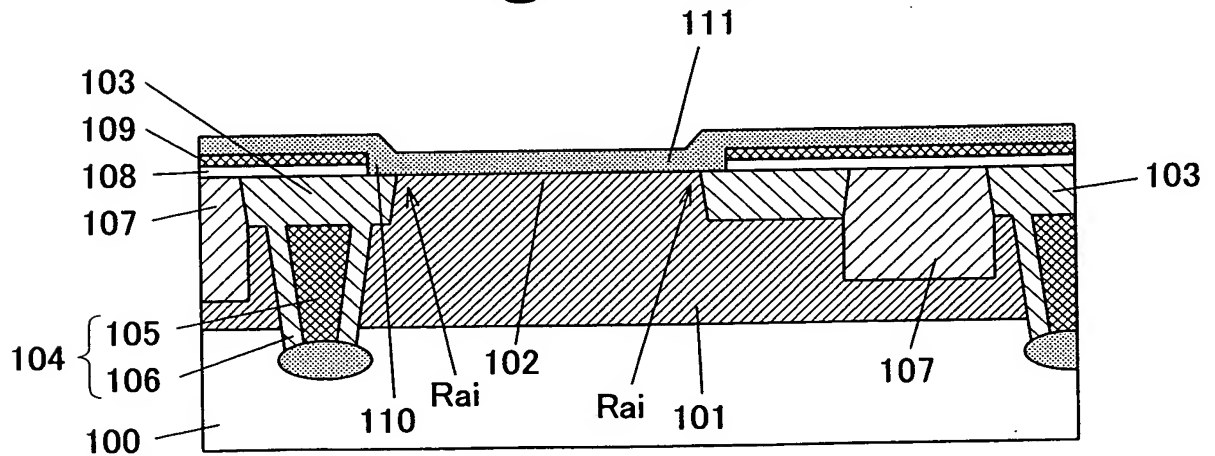


Fig. 1 is a cross-sectional view of a semiconductor device. The device is formed on a substrate 100. A base layer 101 is formed on the substrate 100. A patterned layer 102 is formed on the base layer 101. A top layer 103 is formed on the patterned layer 102. A central region 110 is defined by a trench 107 and a layer 111. A contact 105 is formed in a via 106. A layer 200 is formed on top of the device.

[illegible]



[illegible][illegible]

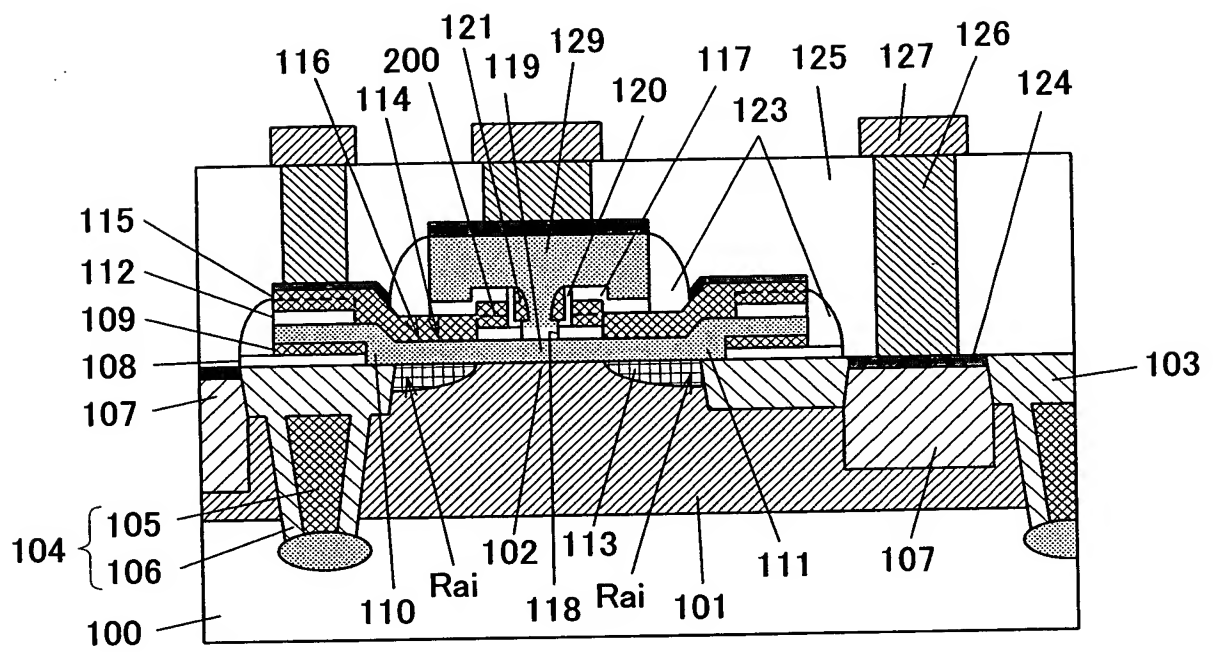


Fig. 5(j)

Fig. 6(a) PRIOR ART

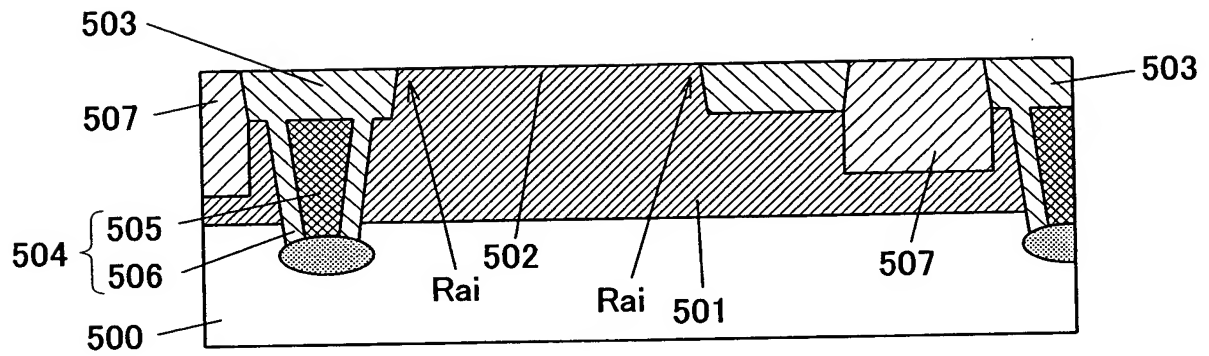


Fig. 6(b) PRIOR ART

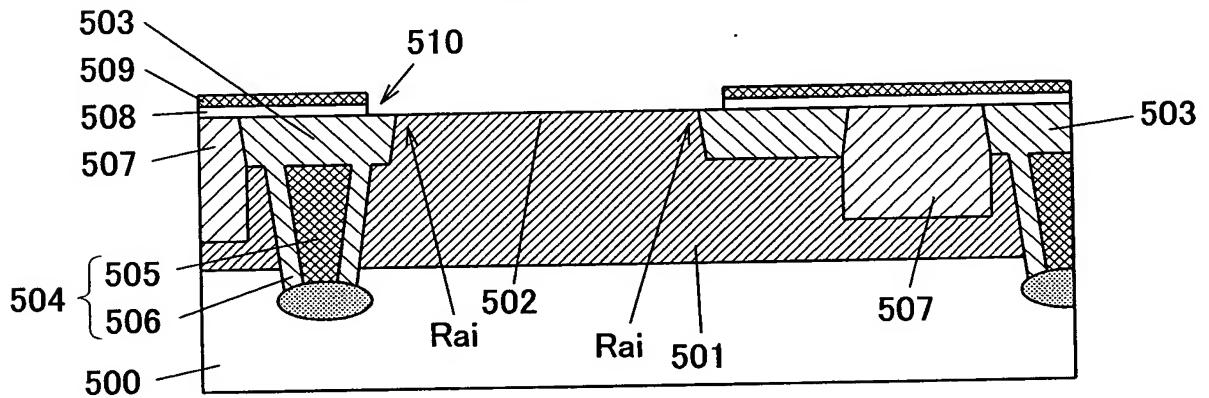


Fig. 6(c) PRIOR ART

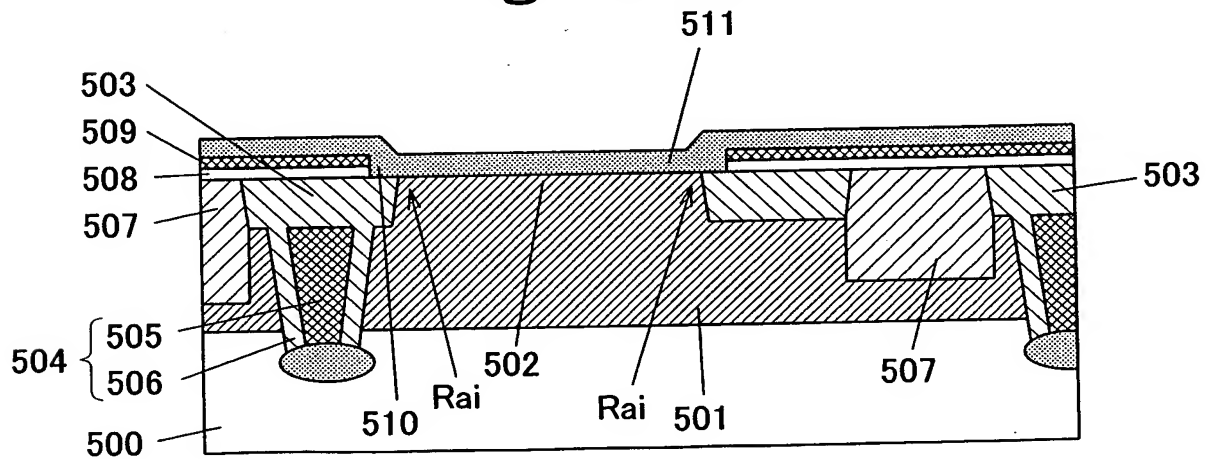


Fig. 7(d) PRIOR ART

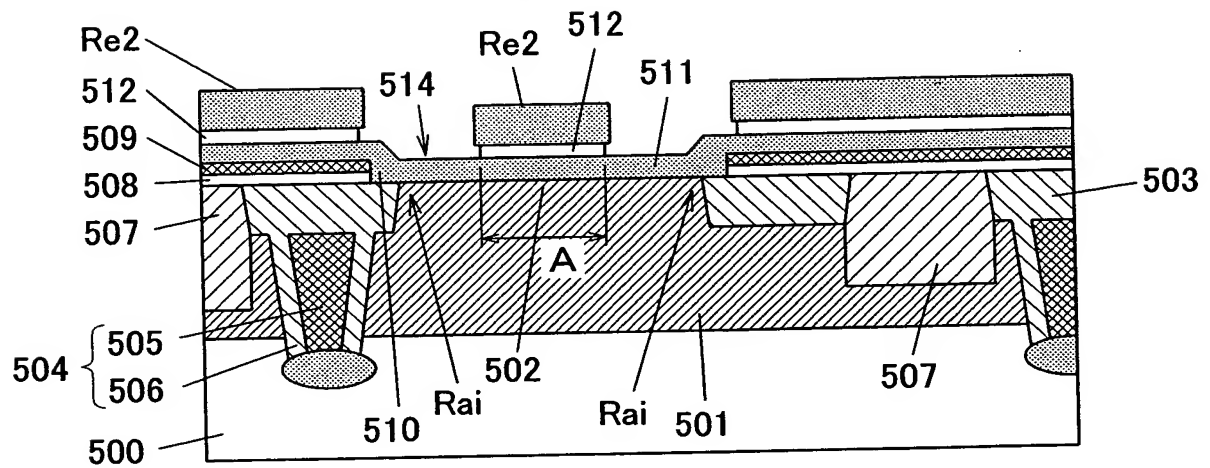


Fig. 7(e) PRIOR ART

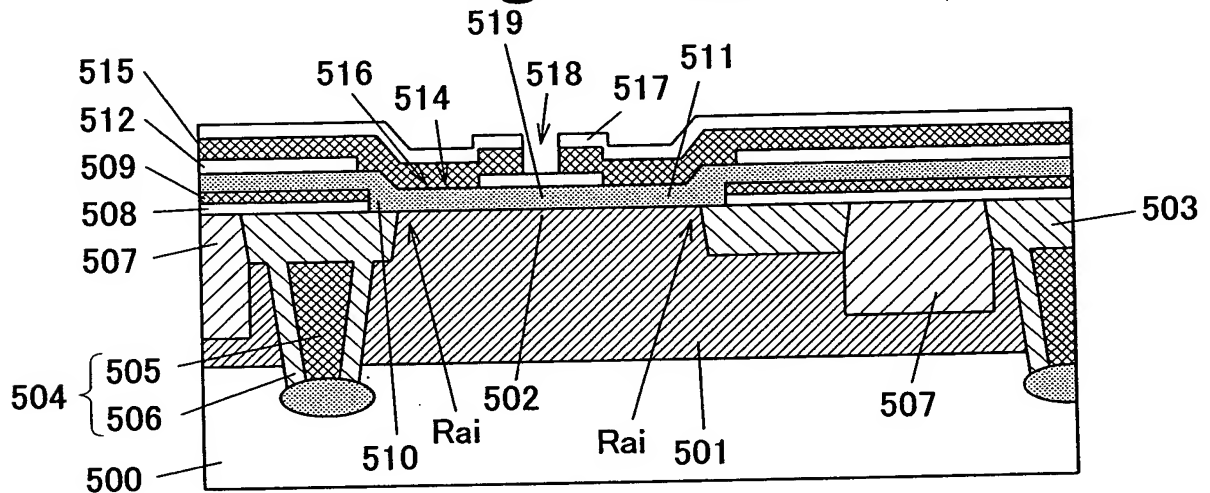
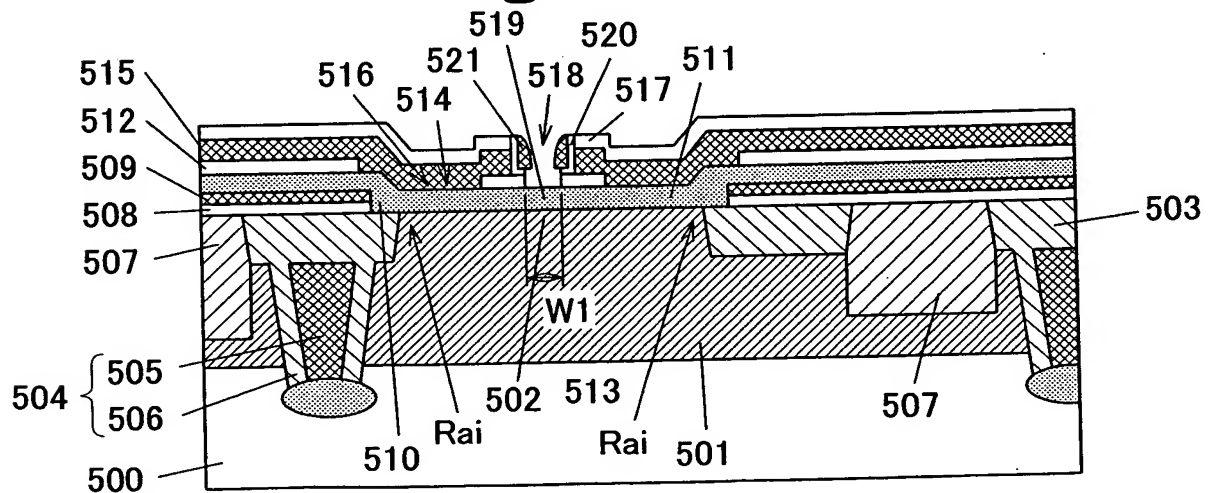


Fig. 7(f) PRIOR ART



[illegible][illegible]

Fig. 1 is a cross-sectional view of a semiconductor device. It shows a substrate 500 with a base layer 501. A central region 502 is surrounded by a ring 503. A top layer 504 contains a central block 505 and side blocks 506. Various other layers and structures are labeled with numbers 507 through 523.



**Fig. 9 (j) PRIOR ART**